

FIG. 1
(Background Art)

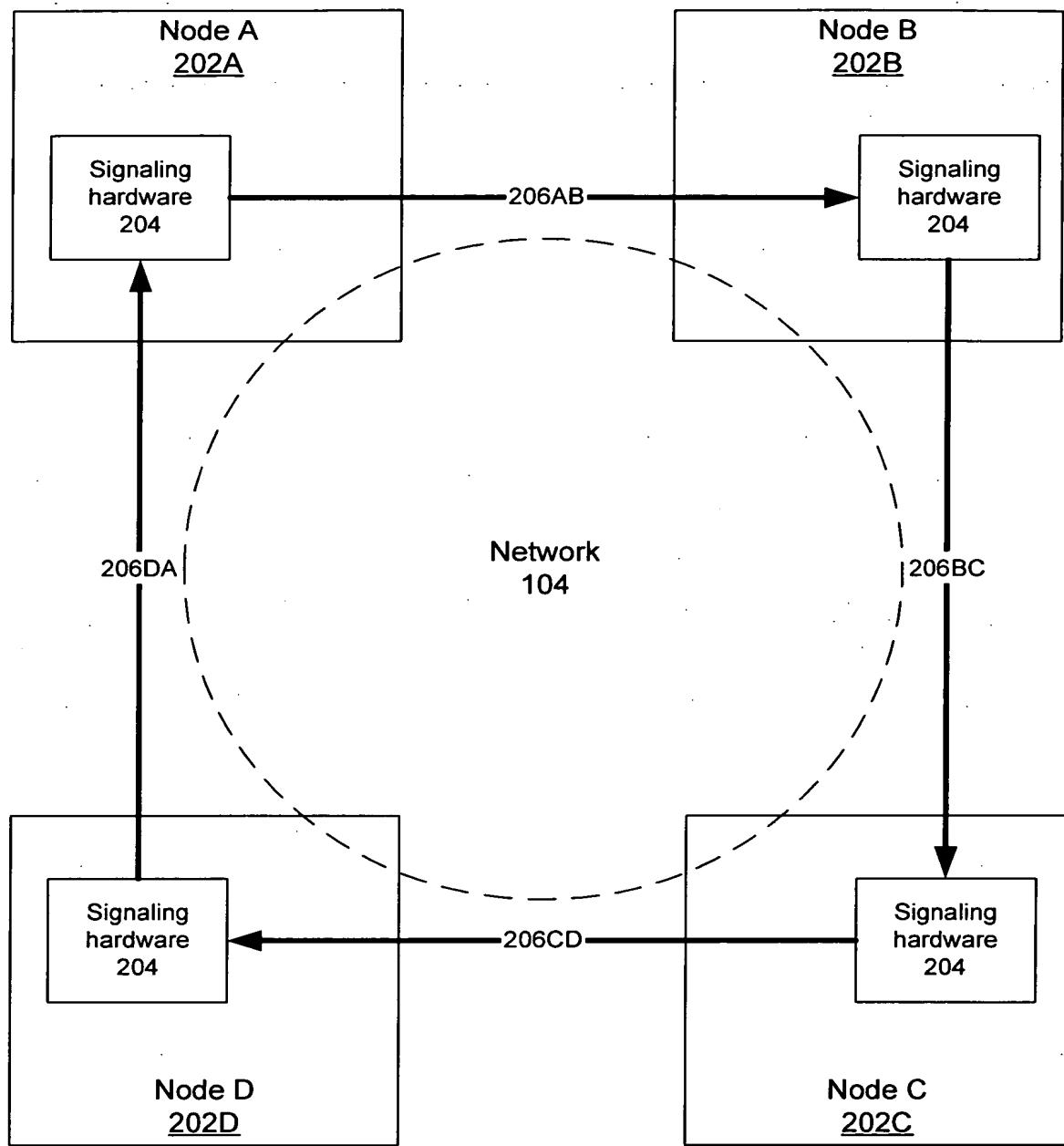
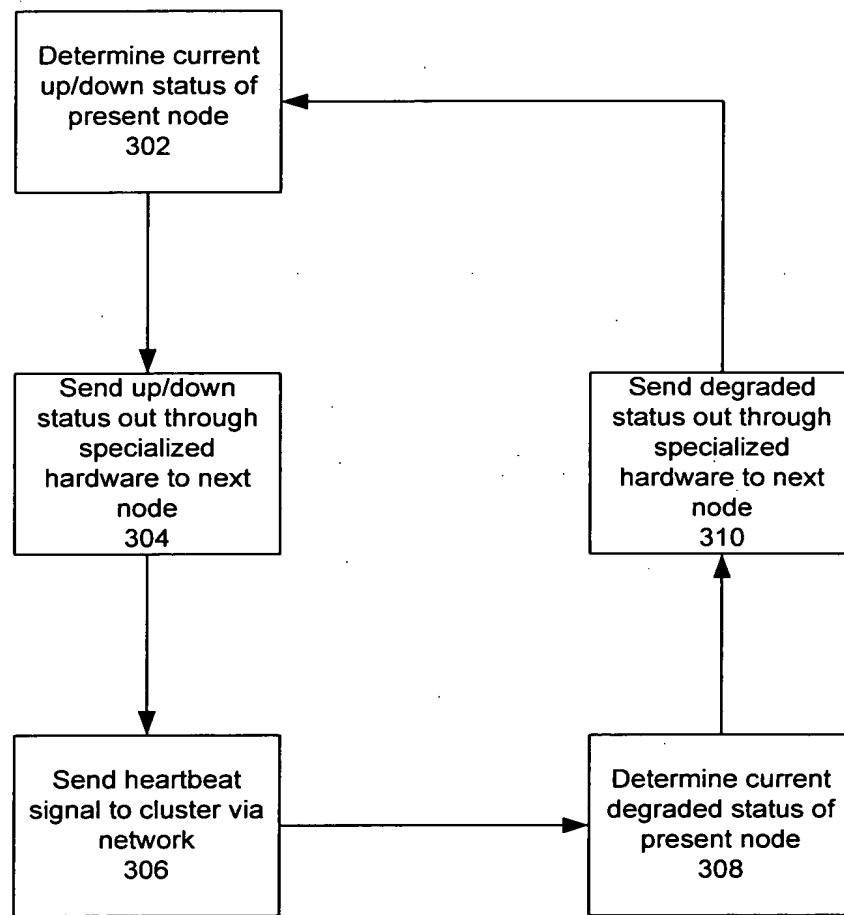


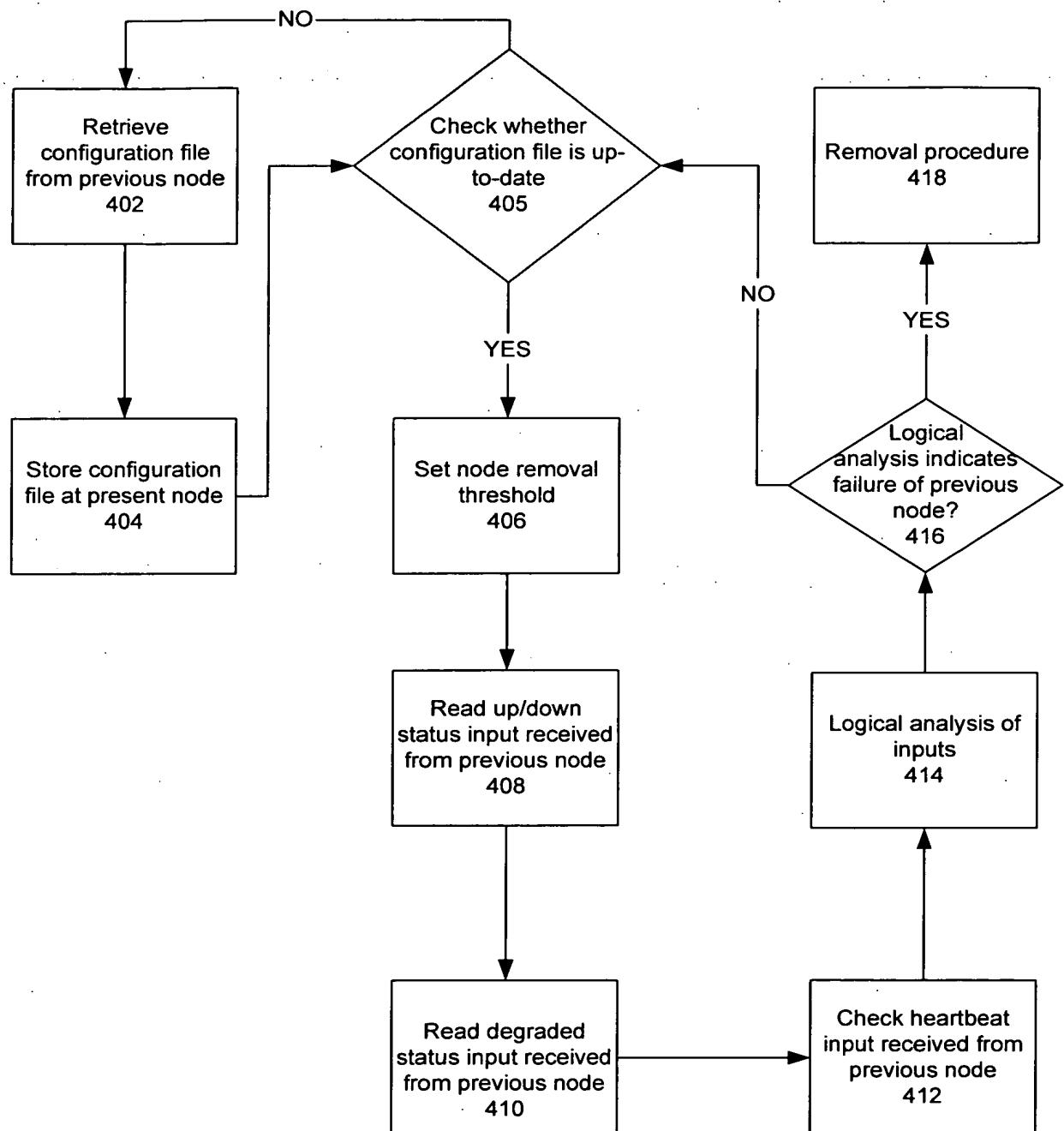
FIG. 2

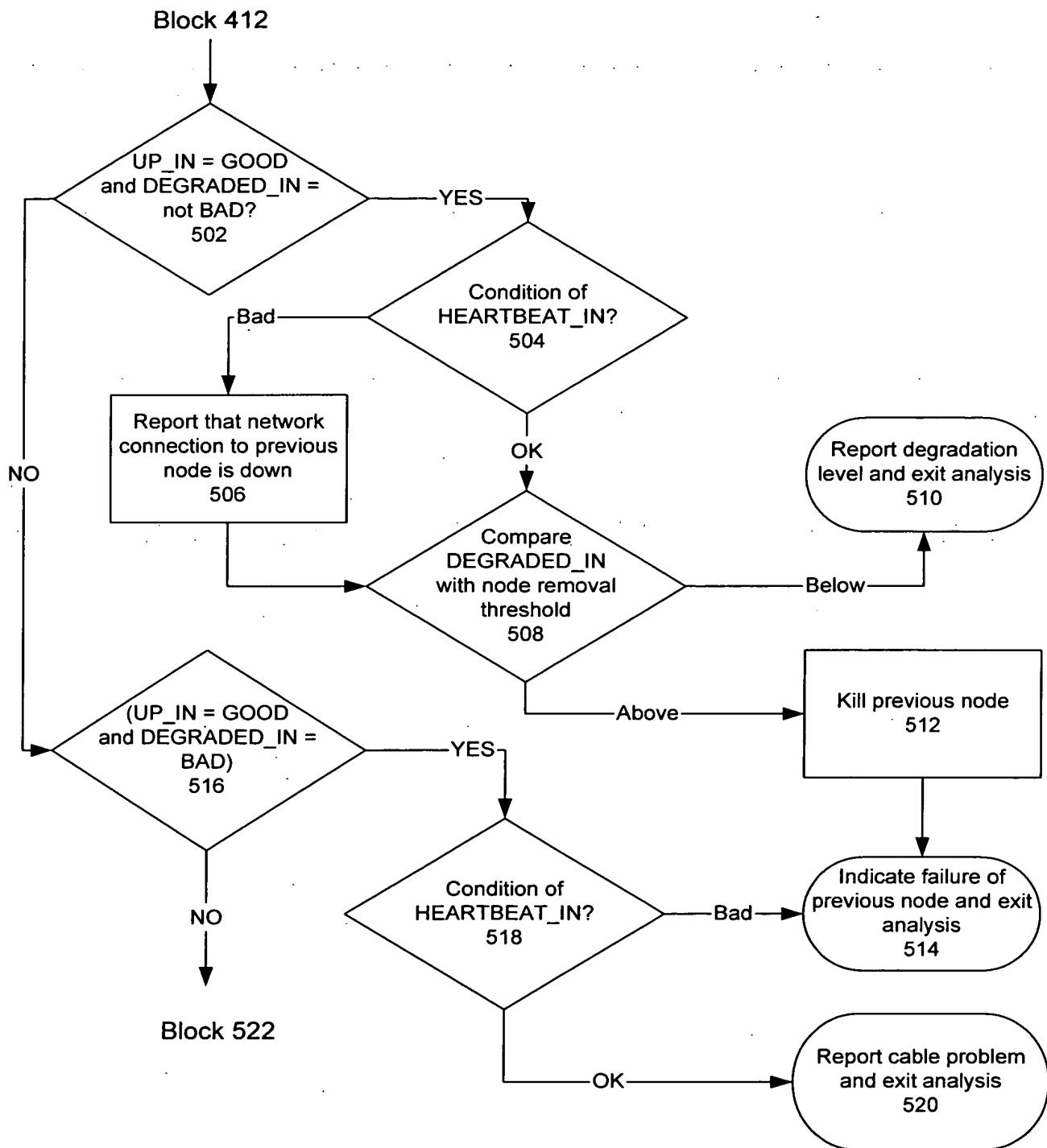
200



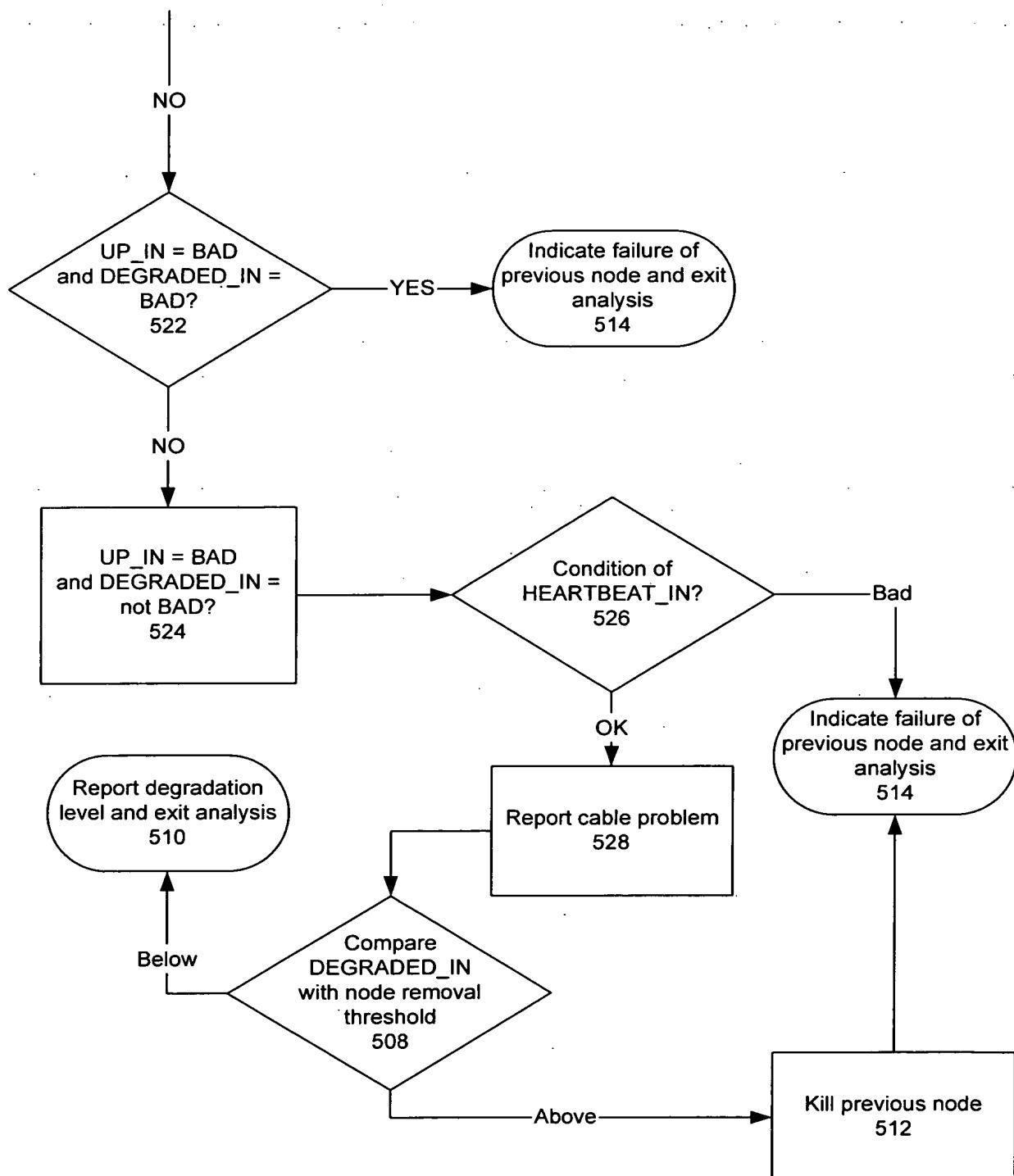
Node Status Generation
Process
300

FIG. 3





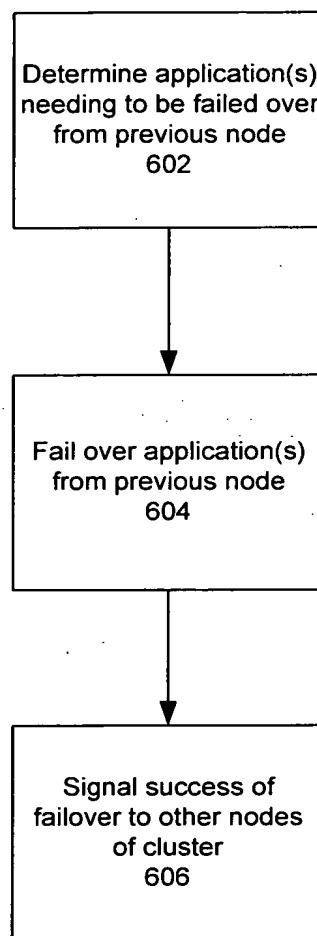
Block 516



Logical Analysis

414

FIG. 5B



Removal Procedure

FIG. 6

418